GAL22LV10

Low Voltage E²CMOS PLD Generic Array Logic™

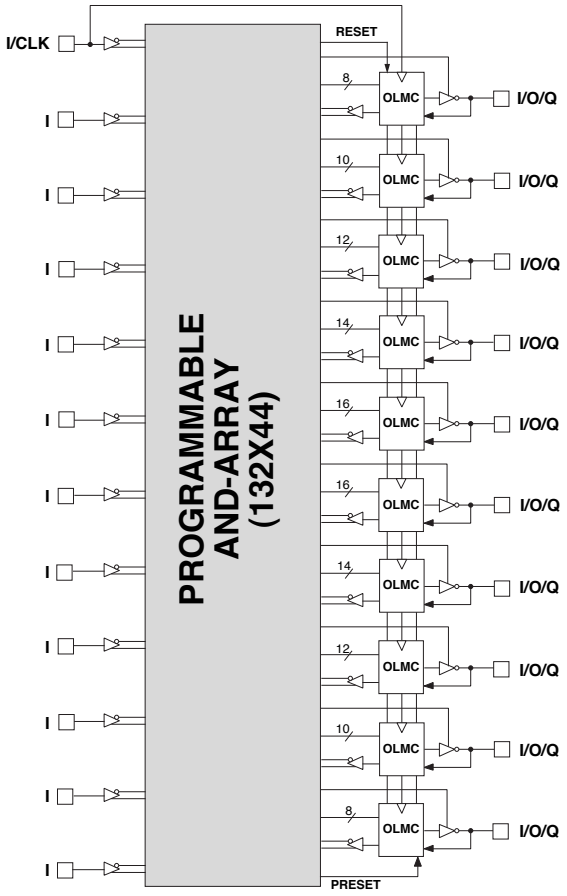
New 5V Tolerant Inputs on 22LV10D

Select devices have been discontinued. See Ordering Information section for product status.

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - 4 ns Maximum Propagation Delay
  - Fmax = 250 MHz
  - 3 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- **3.3V LOW VOLTAGE 22V10 ARCHITECTURE**
  - JEDEC-Compatible 3.3V Interface Standard
  - 5V Compatible Inputs
  - I/O Interfaces with Standard 5V TTL Devices (GAL22LV10C)
- **ACTIVE PULL-UPS ON ALL PINS (GAL22LV10D)**
- **E² CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - Glue Logic for 3.3V Systems
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **LEAD-FREE PACKAGE OPTIONS**

Functional Block Diagram



Description

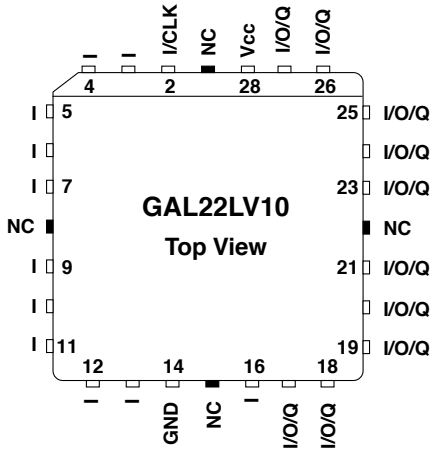
The GAL22LV10D, at 4 ns maximum propagation delay time, provides the highest speed performance available in the PLD market. The GAL22LV10C can interface with both 3.3V and 5V signal levels. The GAL22LV10 is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



LATTICE SEMICONDUCTOR CORP

GAL22LV10 Ordering Information

Conventional Packaging
Commercial Grade Specifications

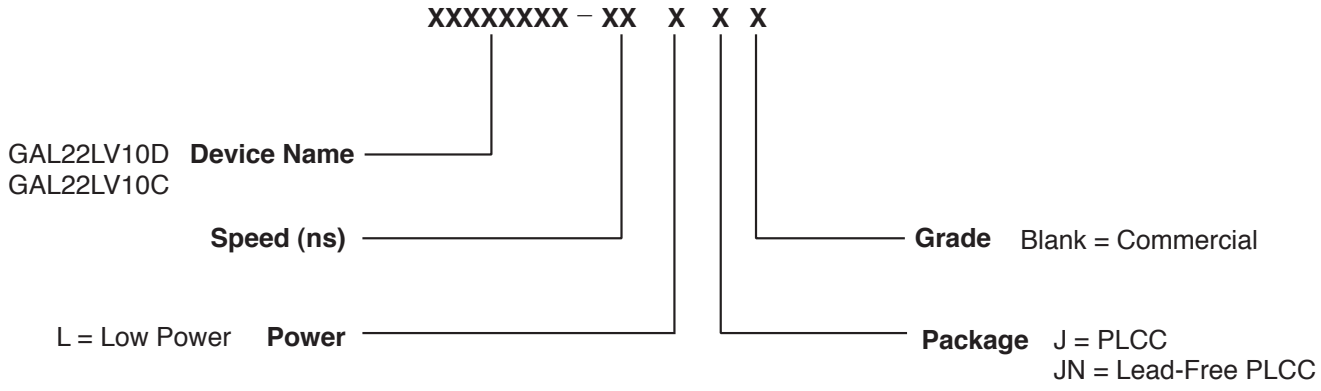
Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
4	3	3	130	GAL22LV10D-4LJ	28-Lead PLCC
5	3.5	3.5	130	GAL22LV10D-5LJ	28-Lead PLCC
7.5	6.5	5	75	GAL22LV10C-7LJ[1]	28-Lead PLCC
10	7.5	6.5	75	GAL22LV10C-10LJ	28-Lead PLCC
15	10	10	75	GAL22LV10C-15LJ	28-Lead PLCC

Lead-Free Packaging
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
4	3	3	130	GAL22LV10D-4LJN	Lead-Free 28-Lead PLCC
5	3.5	3.5	130	GAL22LV10D-5LJN	Lead-Free 28-Lead PLCC
7.5	6.5	5	75	GAL22LV10C-7LJN[1]	Lead-Free 28-Lead PLCC
10	7.5	6.5	75	GAL22LV10C-10LJN	Lead-Free 28-Lead PLCC
15	10	10	75	GAL22LV10C-15LJN	Lead-Free 28-Lead PLCC

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Part Number Description



Select devices have been discontinued.
See Ordering Information section for product status.

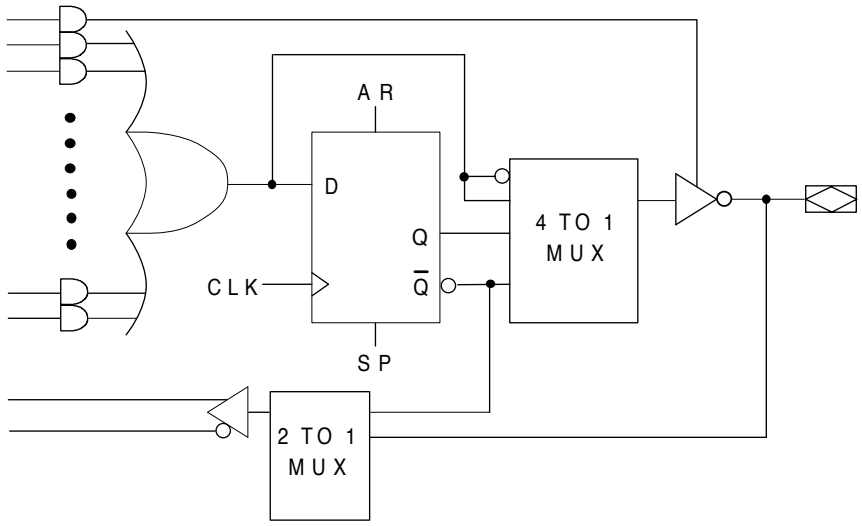
Output Logic Macrocell (OLMC)

The GAL22LV10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 17 and 27), two have ten product terms (pins 18 and 26), two have twelve product terms (pins 19 and 25), two have fourteen product terms (pins 20 and 24), and two OLMCs have sixteen product terms (pins 21 and 23). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22LV10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL22LV10 OUTPUT LOGIC MACROCELL (OLMC)

Output Logic Macrocell Configurations

Each of the Macrocells of the GAL22LV10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... -0.5 to +4.6V
Input voltage applied ..... -0.5 to +5.6V
I/O voltage applied ..... -0.5 to +4.6V
Off-state output voltage applied ..... -0.5 to +4.6V
Storage Temperature .....-65 to 150°C
Ambient Temperature with
Power Applied .....-55 to 125°C

1.Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss - 0.3	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
	I/O High Voltage		2.0	—	Vcc+0.5	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$(Vcc-0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
	Input High Leakage Current	$Vcc \le V_{IN} \le 5.25V$	—	—	10	µA
	I/O High Leakage Current	$Vcc \le V_{IN} \le 4.6V$	—	—	20	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{OL} = 500µA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -100µA Vin = V_{IL} or V_{IH}	Vcc-0.2V	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–8	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A= 25°C	-15	—	-80	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0V V_{IH} = 3.0V Unused Inputs at V_{IL} f_{toggle} = 1MHz Outputs Open	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -4		COM -5		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd[2]	A	Input or I/O to Combinational Output	1	4	1	5	ns
tco[2]	A	Clock to Output Delay	1	3	1	3.5	ns
tcf[3]	—	Clock to Feedback Delay	—	2.5	—	3	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	3	—	3.5	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	167	—	143	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	182	—	154	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	200	—	MHz
twh[4]	—	Clock Pulse Duration, High	2	—	2.5	—	ns
twl[4]	—	Clock Pulse Duration, Low	2	—	2.5	—	ns
ten	B	Input or I/O to Output Enabled	1	5	1	6	ns
tdis	C	Input or I/O to Output Disabled	1	5	1	6	ns
tar	A	Input or I/O to Asynchronous Reset of Register	1	4.5	1	5.5	ns
tarw	—	Asynchronous Reset Pulse Duration	4.5	—	5.5	—	ns
tarr	—	Asynchronous Reset to Clock↑ Recovery Time	3.5	—	4	—	ns
tspr	—	Synchronous Preset to Clock↑ Recovery Time	3.5	—	4	—	ns

1) Refer to **Switching Test Conditions** section.
2) Minimum values for **t**pd and **t**co are not 100% tested but established by characterization.
3) Calculated from **f**max with internal feedback. Refer to **fmax Descriptions** section.
4) Refer to **fmax Descriptions** section. Characterized but not 100% tested.

Capacitance (T_A = 25°C, f = 1.0 MHz)

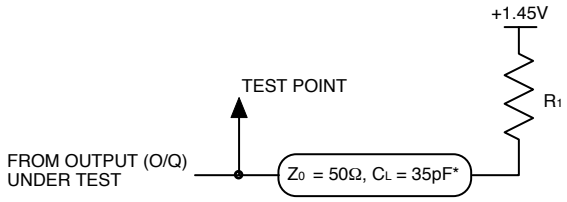
SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_I	Input Capacitance	5	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	5	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

GAL22LV10D: Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Output Load Conditions (see figure)

Test Condition		R_1	C_L
A		50Ω	35pF
B	High Z to Active High at 1.9V	50Ω	35pF
	High Z to Active Low at 1.0V	50Ω	35pF
C	Active High to High Z at 1.9V	50Ω	35pF
	Active Low to High Z at 1.0V	50Ω	35pF



*C_L includes test fixture and probe capacitance.

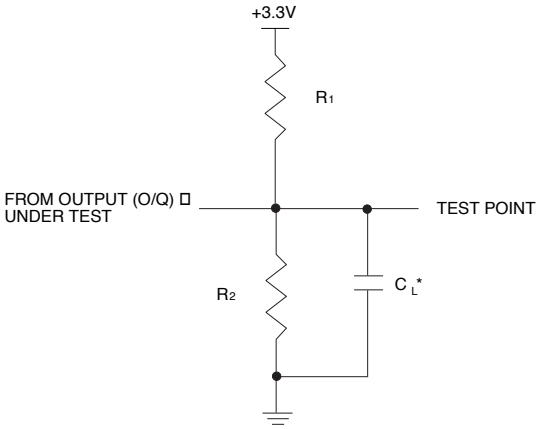
GAL22LV10C: Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2.0ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		316Ω	348Ω	35pF
B	Active High	316Ω	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High	316Ω	348Ω	5pF
	Active Low	316Ω	348Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

Select devices have been discontinued.
See Ordering Information section for product status.